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(54) Method for the production of special wafers made from semiconductor material

(57) This invention relates to a production process for wafers, which are used in the manufacture of electronic components; it offers several advantages compared to conventional wafers, particularly in regard to high-temperature treatment and during structuring of the wafers. The object of the invention is therefore to avoid or at least reduce the negative effects of the temperature field during high-temperature treatment, affecting the physical shape of the wafers during lithography. This problem has been solved by notching a grown mono-crystal in an axial direction according to a certain pattern, then slicing it in a direction which is vertical to its axis (alternatively, the sliced wafers can be notched later, preferably in a radial direction; see FIG. 1). The notched wafers obtained by this process are then polished using a suitable technology and are subjected to a production cycle for manufacturing electronic components. This application is primarily intended for large-diameter silicon wafers, which are used for the production of highly-integrated components.

-Fig. 1-

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Title of the invention

Method for the production of special wafers made from semiconductor material

Field of the invention

This invention relates to a production process for special wafers made from semiconductor material, particularly silicon, which is obtained by a known crystal-growing method in a mono-crystalline, mostly dislocation-free structure and in the form of large cylindrical crystal pieces. Round wafers, having a thickness of some 10^{-1} mm and produced from such crystals, are required for manufacturing electronic components. During the process of manufacturing these electronic components which are usually arranged in large numbers on a single wafer, each wafer is subjected to certain steps of a high-temperature treatment and/or structuring, depending on the technology required for the component.

Description of the Related Art

For economic reasons, these wafers are usually not treated separately in an oxidation or diffusion furnace during the manufacturing process - which would be advantageous in regard to the temperature field - but

are usually arranged in batches, then placed simultaneously in certain intervals in a high-temperature furnace. The wafers are energized by absorbing infrared and visible light from the radiation field of the furnace, whereby the mean temperature of the wafers slowly approaches the temperature of the furnace. During heating and cooling of the wafers a mainly radially oriented heat flow will be created within the wafers, according to the temperature distribution of the wafer; this is caused by the previously described arrangement of the wafers in the furnace. During heating of the wafer, these heat flows are oriented in a negative radial direction, while during cooling they change to a positive radial direction. The prevailing gradients of the temperature field lead to mechanical stress within the wafer, causing harmful effects which increase proportionally with the diameter of the wafer. The larger the diameter of the wafer, the more intense the stress becomes, which has a major influence on the geometric and structural resistance of the wafer. After some high-temperature treatment steps, the wafers are showing structural defects (such as dislocations, stacking faults) in disturbing concentrations and arrangements, as well as lasting deformations, caused by mechanical stress

effects. Several methods have been tried to secure the high-temperature resistance of the wafers, such as special polishing techniques, optimum furnace temperature profiles, defined charging (inserting and removing the wafers to/from the furnace), adding certain doping agents (O, H, B) during crystal growing, as well as low-temperature oxidation. Nevertheless, there is no known fully satisfying solution to the problem of high-temperature resistance on large-diameter wafers.

During lithographic processes, particularly during photolithography, the above mentioned deformations, faults or rough spots on the wafer surface may have a detrimental effect on the sharpness of the image, i.e. the structuring; this applies especially to the contact lithography process. However, the tendency towards a total integration of components not only makes it necessary to maintain the current standard of sharpness, but to improve it. For this reason it becomes more and more troublesome if rough spots and deformations of the wafer occur during one of the technological production steps. The dimensional stability of the wafers during the entire technological production sequence of the high-temperature treatment and/or the lithographic process is - at the current state of technology - by no means guaranteed,

particularly since the demand is rising for wafers with larger diameters. It is for these reasons that this invention uses a different approach.

Object of the invention

It is an object of an invention to develop a method which allows the production of special wafers, made of semiconductor material, which exhibit more advantageous characteristics during high-temperature treatment and during structuring, leading to a significant reduction in rejects by employing this new method.

Summary of the Invention

It is the object of the invention to diminish or eliminate the effects of the temperature field within the volume of the wafers, qualitatively described above, which affects the shape and amount of defects, as well as reducing the defect structure and the negative effects it has on the real shape of the wafers, which influences the structuring sharpness during lithographic processes, particularly during photolithography. This objective is reached in the sense of the invention by employing an innovative manufacturing process for producing special wafers; this process consists largely

of a series of generally known procedure steps used in growing crystals, separating crystals, etching, as well as, for example, temper-hardening, thermal oxidation and/or diffusion. Improved characteristics of the wafers during the production of semiconductor components are obtained by

- growing a basically cylindrical mono-crystal made from semiconductor material by a known crystal-growing method, then making one or more incisions according to a certain system and in an axial direction, from the crystal shell to a certain depth, without cutting completely through the wafer;
- arranging the slit mono-crystal in such a way that it can be cut up at an angle approaching more or less 90° to the axial direction, resulting in sliced and slit wafers,

or

- using instead cut wafers from a grown, arranged mono-crystal made from semiconductor material, making incisions at an angle approaching more or less 90° to the axial direction, according to a certain system and in a vertical direction to the wafer surface, cutting from the wafer edge

to a certain depth, but without cutting completely through the wafer,

and

- processing the slit wafers in each case by using generally known processing steps designed for such wafers, such as etching, mechanical and/or chemical-mechanical polishing, in order to obtain polished wafers,
- subjecting the polished wafers to a certain technological processing cycle, which includes high-temperature treatment and/or structuring (such as temper-hardening, oxidation, out-diffusion, in-diffusion, photolithography, etc.), then separating the structured wafers at the end of the processing cycle for optimum surface utilization, using abrasive cutting, notching and breaking, laser cutting, etc., in order to obtain separate components, which then can be bonded and encapsulated.

In accordance with the object of the invention, it is advantageous to make the incisions in the direction of the heat flows, which are generated during high-temperature treatment, that is, in a radial direction.

It is also in accordance with the object of the invention that, when determining the incision system, the symmetry of the voltage tensor, the generally rectangular shape of the component, and the crystallographic symmetry of the wafer must be taken into account; this means that preferably radial incision systems of a fourfold coordination should be used. In some cases an arranged radial incision will be sufficient to ensure that the improved characteristics of the wafer will be effective. If additional technical parameters are taken into consideration, non-radial incision systems may also be advantageous. Preferred directions for these incision systems are <211> for wafers with a (111) orientation, and <100> and <110> respectively for wafers with a (100) orientation.

In accordance with the described procedure it is preferable to remove sufficient material from the immediate incision area to ensure that the depth of interference caused by abrasive cutting is smaller than the thickness of the layer removed by etching, and that the mono-crystal or the wafer is heated only after the disturbed layer has been removed by an etching process. If this is not done, the surface defects of the crystal lattice (primarily dislocations) will be transferred to the wafer volume. Since it is technically less

difficult to make the incisions on the mono-crystal first, and then slice the mono-crystal into wafers, it would be advantageous to make sufficiently wide incisions on the grown mono-crystal, to enable an unobstructed area of attack for the etching agent, in order to ensure complete removal of the damaged layer, and then to etch the cut wafers, concluding with a mechanical/chemical-mechanical polishing process. This method ensures that the breaking-off of small pieces of material in the incision area which can cause scratches and abrasions during polishing of the wafer surface is effectively prevented. The invention is explained in the next chapter, using a simple embodiment.

Embodiment

FIG. 1 shows a diagram of a cut silicon wafer 1, produced according to the invention process (since the materials used for production as well as further processing and control procedures are part of the current state of technology, it is not necessary to illustrate such materials and steps). Wafer 1 has a diameter of 100 mm and a thickness of about 500 μm; it was cut by means of an inboard abrasive cutter from a CHOCHRALSKI-drawn silicon mono-crystal - known to be of the diamond lattice type - which was cut lengthwise with

an outboard abrasive cutter. Orientation of the surface normal line on the wafer runs approximately in the <111> direction, and the material is boron-doped from 4 to 8 Ω·cm. In the lower area of the wafer, chamfer 2 can be seen; normally, this cut is made on the mono-crystal before slicing, in order to facilitate the crystallographic orientation on the wafer. Starting from the center of chamfer 2 - that is, in a <110> direction, and offset by 90° each - four radial incisions 3, 4, 5 and 6 are made, which are each 25 mm deep and 1 mm wide; they represent the incision system and divide wafer 1 into the four sectors 7, 8, 9 and 10. The edges of the incisions 3, 4, 5 and 6, shown in FIG. 1 as borders, and the corners 11, 12, 13, 14, 15, 16, 17 and 18 are rounded off during the etching, prior to the polishing process. Under these conditions, the interference depth amounts to less than 20 μm. Correspondingly, the thickness of wafer 1 will be 400 μm after etching, and 380 μm after polishing. The incisions will widen to approximately 1,2 mm, since the slowest rate of material reduction will occur in the <111> direction. The polished wafer will be subjected to thermal oxidation at approximately 1450 K. The measured radii of curvature are on average considerably larger than for wafers having no incisions, made from

the same material and using current technology. Correspondingly, the structuring within the sectors 7, 8, 9 and 10 can be performed with the necessary precision; in addition, the remaining inaccuracies of the wafer shape exert only a minor influence, since the wafer produced according to the invention can be fitted more precisely during fixation for photolithographic processing. At the end of the so-called cycle I, which includes the high-temperature treatment to produce the actual electronic structures on the wafer, separation is performed by means of outboard abrasive cutting.

When using a different process in the sense of the invention, the incisions 3, 4, 5 and 6 can be made with varying depths; incision 3 in FIG. 1 could be extended to reach the center of the wafer, and incisions 4, 5 and 6 could be eliminated. Even with this modified incision system, reduced to just one incision, the projected advantages can be realized. The cutting effort is in this case particularly small, and there is minimal loss of structurable area. Since the incision itself makes orientation on the wafer possible, chamfering is probably not required when making incisions of variable depths or when using only one incision. This eliminates the processing steps and problems which occur during chamfering.

What is claimed is;

1. A method for producing special wafers made from semiconductor material; the production process includes already known manufacturing steps used in crystal growing, crystal separation, etching, mechanical and/or chemical-mechanical polishing, as well as temper-hardening, oxidation and/or diffusion,
characterized by

- growing a basically cylindrical mono-crystal made from semiconductor material by a known crystal-growing method, then making one or more incisions according to a certain system and in an axial direction, from the crystal shell to a certain depth, without cutting completely through the wafer;

- arranging the slit mono-crystal in such a way that it can be cut up at an angle approaching more or less 90° to the axial direction, resulting in sliced and slit wafers,

or using instead cut wafers from a grown, arranged mono-crystal made from semiconductor material, making incisions at an angle approaching more or less 90° to the axial direction, according to a certain system and in a vertical direction to the wafer surface, cutting from the wafer edge to a certain depth, but without cutting completely through the wafer,

and processing the slit wafers in each case by using generally known processing steps designed for such wafers, such as etching, mechanical and/or chemical-mechanical polishing, in order to obtain polished wafers,

and subjecting the polished wafers to a certain technological processing cycle, which includes high-temperature treatment and/or structuring (such as temper-hardening, oxidation, out-diffusion, in-diffusion, photolithography, etc.), then separating the structured wafers at the end of the processing cycle for optimum surface utilization, using abrasive cutting, notching and breaking, laser cutting, etc., in order to obtain separate components which then can be bonded and encapsulated.

2. Method according to Claim 1, characterized in that the incisions on the mono-crystal or the wafer are made in such a way that they correspond to the temperature field which is representative for the respective high-temperature treatment, that is, the incisions are arranged in the direction of the temperature gradient.

3. Method according to Claim 2, characterized in that the incisions are made in a radial direction.

4. Method according to Claim 1 or 3, characterized in that the incisions are made in a vertical direction to each other.

5. Method according to Claim 1 or 2, characterized in that the system of incisions (or the single incision) is made according to certain crystallographic arrangements.

6. Method according to Claim 5, characterized in that one of the incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <111> orientation, is made in a <211> direction.

7. Method according to Claim 5, characterized in that one of the incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <111> orientation, is made in a <110> direction.

8. Method according to Claim 5, characterized in that incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <100> orientation, are made in <100> directions.

9. Method according to Claim 5, characterized in that incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <100> orientation, are made in <110> directions.

10. Method according to Claims 4 and 6, characterized in that one of the four incisions on

wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <111> orientation, is made in a <211> or <110> direction respectively.

11. Method according to Claim 4 and 8 or 4 and 9, characterized in that incisions on wafers, which are obtained from a grown diamond-lattice type mono-crystal with a <100> orientation, are made in <100> or <110> directions respectively.

12. Method according to Claim 1, characterized in that the reference direction for technological processes, such as during structuring of the wafer, is based on the incision system or a single incision instead of a chamfer.